

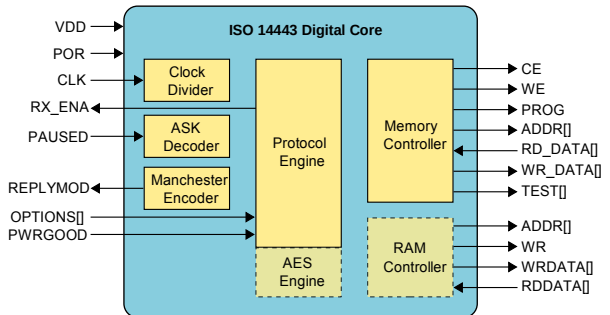
ISO 14443 Digital Core

Overview

RADLogic's **ISO 14443 Digital Core** IP Block is a low-power, low-area HDL digital core for proximity RFID systems compatible with the ISO/IEC 14443-3 standard (Type A) and supports NFC applications when the memory is configured with suitable data structures.

Features

- **Clock Divider:** Performs division and gating of the master clock for use by other modules in the core.
- **ASK Decoder:** Decodes the Modified Miller ASK data signal demodulated by the AFE and delivers the command bits one at a time to the Protocol Engine.
- **Manchester Encoder:** Encodes the reply data-stream using OOK subcarrier for transmission by the AFE
- **Protocol Engine:** Implements all of the mandatory commands required by the ISO 14443-3 Type A standard as well as custom memory access commands with page locking features and can easily be extended to support additional functionality. Supported commands: *SEL*, *REQA*, *HALT*, *WUPA*, *READ*, *WRITE*.
- **Memory Controller:** Provides a generic memory interface layer which allows it to interface to a wide variety of different memory IP blocks.
- **Optional AES Engine and RAM Controller:** Implement custom AES_ENCRYPT and AES_READ commands which can be used for e.g. tag authentication.



Specifications

- Supply voltage 0.8 to 1.8v.
- 13.56 MHz master clock (carrier) frequency.
- Current consumption <10uA at VCC=1.6V .
- Size ~30,000um² in 180nm technology / ~3,600 gates equiv. (dep. on options), add ~16,000um² / ~2,000 gates for AES Engine and RAM Controller.
- Technology independent Verilog HDL.
- Custom features (such as password protection), commands and interfaces (e.g. I2C, GPIO, UART etc.) can easily be added to suit application needs.
- The ISO14443 digital core is designed to be paired with RADLogic's analog front end and suitable memory for storage of data.

Technologies

Technology independent soft core, portable to any suitable cell library.

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RADLogic Pty Ltd

Suite 4, 15 Fullarton Road, Kent Town, South Australia A 5067, Australia
 t: +61 8 8362 3255 email: info@radlogic.com www.radlogic.com