RADLogic
Research, Analysis and
Design of Integrated
Circuits and Systems

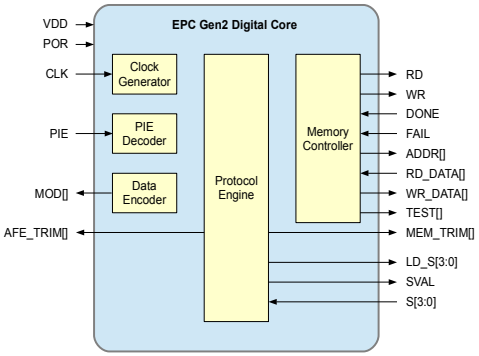
EPC Gen2 Digital Core

Overview

RADLogic's **EPC Gen2 Digital Core** IP Block is a low-power, low-area HDL digital core for UHF RFID systems compatible with EPCGlobal Class 1 Gen2 / ISO18000-6C standards.

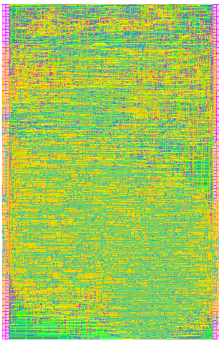
Features

- **Clock Generator**: Performs division and gating of the master clock for use by other modules in the core.
- **PIE Decoder**: Decodes the PIE data signal demodulated by the AFE and delivers the command bits one at a time to the Protocol Engine.
- **Data Encoder**: Encodes the reply data-stream using either FM0 or Miller encoding.
- **Protocol Engine**: Implements all of the mandatory and optional commands required by the EPC Gen2 v1.2 standard, and can easily be extended to support additional features from v2.0. Also, includes proprietary commands for memory testing.
- **Memory Controller**: Uses a generic handshake-based approach to allow it to interface to a wide variety of different memory IP blocks.



Specifications

- Supply voltage 0.8 to 1.8v
- 2MHz master clock frequency
- Current consumption ~5uA
- Size ~0.1mm^2 (depending on options)
- Technology independent HDL (Verilog or VHDL)
- All commands fully implemented, including optional Access and BlockWrite commands.
- Custom commands can easily be added to suit application needs.
- The EPC Gen2 digital core is designed to be paired with RADLogic's RF front end and suitable memory for storage of data and persistence bits.



Technologies

Technology independent soft core, portable to any suitable cell library.

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