EPC Gen2 Verification Platform

Test Vector Generation Suite

Interactive GUI
Allows Interactive Development of Test Vector "Packet Files" and allows users to compose commands and "see" the responses and the effect on state and memory contents.

Verification Vector Suite
"Test Scripts" written using the Python language, that interact with the Behavioural Model to generate "Packet Files" that can be applied to the Test Bench that exercises the DBB. The scripts have been developed to exercise the logic and its timing to cover the conformance requirements specified in "EPC™ Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Conformance Requirements Version 1.0.4"
This vector set covers functionality of EPC Spec version 1.09 and the timing requirements for all versions of the spec, and also the Optional BlockPermalock command of Version 1.2.0 of the EPC spec.

User Verification Suite
Customer Developed "Test Scripts"

EPC Behavioural Model
A high level model of the Digital Protocol Engine Functionality

Verification Packet Files Suite
This is the Verification Vector Suite, converted to Packet Files using the Behavioural Model.
The Packet Files contain listings of commands, expected responses and response timing windows, interspersed with simulation control directives that help to control the testbench.

Simulation TestBench (SystemVerilog)
Incorporates simplified model of a Reader
Interprets packet files, applies commands and outputs responses and timing to "Result Packet Files". Also generates a log file which may contain additional run-time errors such as CRC mismatch, AFE or Memory errors, etc

EPC Gen2 Chip HDL Model

AFE Digital Model (SystemVerilog)
A simplified, Behavioural AFE model designed to pass Testbench signals to/from the logic (an example is provided by RADLogic, and can be substituted by a customer model)

Digital Logic Core
RTL or Gate Level Implementation of the protocol engine, Including Memory Model (Provided by the Customer or RADLogic)

Memory Model
Behavioural or RTL model of the NVM.
(Provided by IP vendor)

Logic Simulator
Compiles and Simulates the Test-bench and Chip Model together.

Result Packet Files
Listings of commands, actual responses and response timings

Filtering and Comparison
Checks that reply timing falls between specified timing windows and filters out "random number" values, which may differ between Behavioural model and the Implementation.

Comparison Results

- Provided by RADLogic
- Provided by Customer or RADLogic
- Provided by Customer or Third Party
- Verification Outputs
- Optional Features

© RADLogic 2015

RADLogic Pty Ltd, Suite 4, 15 Fullarton Road, Kent Town South Australia, AUSTRALIA, www.radlogic.com.au, email: info@radlogic.com.au