Test Vector Generation Suite

Interactive GUI
Allows Interactive Development of Test Vector “Packet Files” and allows users to compose commands and “see” the responses and the effect on state and memory contents.

Verification Vector Suite
“Test Scripts” written using the Python language, that interact with the Behavioural Model to generate “Packet Files” that can be applied to the Test Bench that exercises the DBB. The scripts have been developed to exercise the logic and its timing to cover the conformance requirements specified in “EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Conformance Requirements Version 1.0.4”
This vector set covers functionality of EPC Spec version 1.09 and the timing requirements for all versions of the spec, and also the Optional BlockPermalock command of Version 1.2.0 of the EPC spec.

User Verification Suite
Customer Developed “Test Scripts”

EPC Gen2 Chip HDL Model

AFE Digital Model (SystemVerilog)
A simplified, Behavioural AFE model designed to pass Testbench signals to/from the logic (an example is provided by RADLogic, and can be substituted by a customer model)

Digital Logic Core
RTL or Gate Level Implementation of the protocol engine, Including Memory Model (Provided by the Customer or RADLogic)

Memory Model
Behavioural or RTL model of the NVM. (Provided by IP vendor)

EPC Behavioural Model
A high level model of the Digital Protocol Engine Functionality

EPC Gen2 Verification Platform

Provided by RADLogic
Provided by Customer or RADLogic
Provided by Customer or Third Party
Verification Outputs
Optional Features

Logic Simulator
Compiles and Simulates the Testbench and Chip Model together.

Result Packet Files
Listings of commands, actual responses and response timings

Filtering and Comparison
Checks that reply timing falls between specified timing windows and filters out “random number” values, which may differ between Behavioural model and the Implementation.

Comparison Results

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